

# OPTIREG™ linear TLE42744GV50

## 5 V low dropout linear voltage regulator



### Features

- Very low current consumption
- Output voltages 5 V  $\pm 2\%$
- Output current up to 400 mA
- Very low dropout voltage
- Output current limitation
- Reverse-polarity protection
- Overtemperature shutdown
- Wide temperature range from  $-40^{\circ}\text{C}$  up to  $150^{\circ}\text{C}$
- Green Product (RoHS-compliant)



### Potential applications

- Suitable for use in automotive electronics

### Product validation

Qualified for automotive applications. Product validation according to AEC-Q100.

### Description

The OPTIREG™ linear TLE42744GV50 is a monolithic integrated low dropout voltage regulator for load currents up to 400 mA. An input voltage up to 40 V is regulated to  $V_{Q,nom} = 5\text{ V}$  with a precision of  $\pm 2\%$ . The device is designed for the harsh environment of automotive applications. Therefore, it is protected against overload, short-circuit, and overtemperature conditions by the implemented output current limitation and the overtemperature shutdown circuit. The TLE42744GV50 can be also used in all other applications requiring a stabilized 5 V voltage.

Due to its very low quiescent current, the TLE42744GV50 is dedicated for use in applications permanently connected to  $V_{BAT}$ .

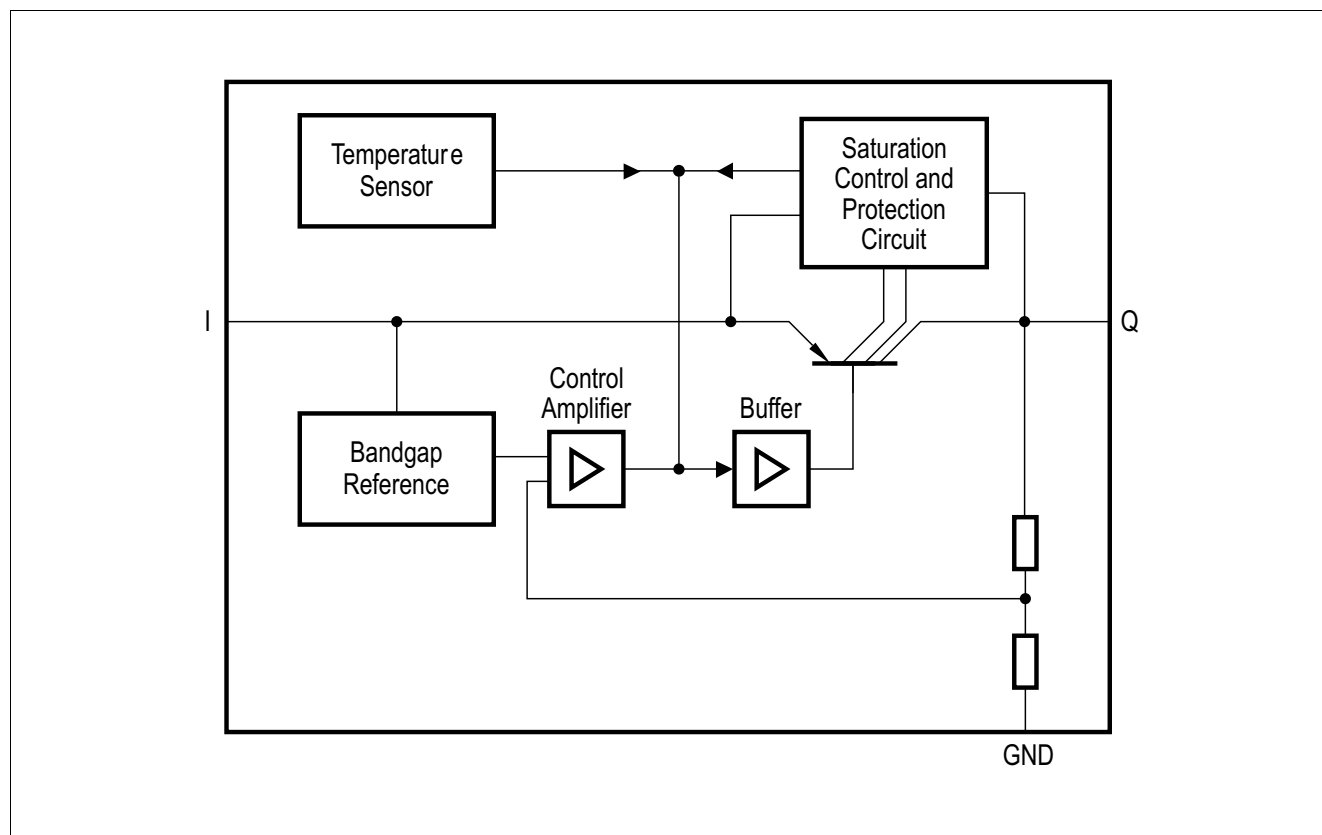
Type	Package	Marking
TLE42744GV50	PG-TO263-3	42744V5

## Table of contents

	<b>Features</b>	<b>1</b>
	<b>Potential applications</b>	<b>1</b>
	<b>Product validation</b>	<b>1</b>
	<b>Description</b>	<b>1</b>
	<b>Table of contents</b>	<b>2</b>
<b>1</b>	<b>Block diagram</b>	<b>3</b>
<b>2</b>	<b>Pin configuration</b>	<b>4</b>
2.1	Pin assignment	4
2.2	Pin definitions and functions	4
<b>3</b>	<b>General product characteristics</b>	<b>5</b>
3.1	Absolute maximum ratings	5
3.2	Functional range	6
3.3	Thermal resistance	6
<b>4</b>	<b>Electrical characteristics</b>	<b>7</b>
4.1	Electrical characteristics of the voltage regulator	7
<b>5</b>	<b>Typical performance characteristics</b>	<b>8</b>
5.1	Typical performance characteristics of the voltage regulator	8
<b>6</b>	<b>Application information</b>	<b>10</b>
6.1	Selection of external components	10
6.1.1	Input pin	10
6.1.2	Output pin	10
6.2	Thermal considerations	11
6.3	Reverse polarity protection	12
6.4	Further application information	12
<b>7</b>	<b>Package information</b>	<b>13</b>
<b>8</b>	<b>Revision history</b>	<b>14</b>

## Block diagram

### 1 Block diagram

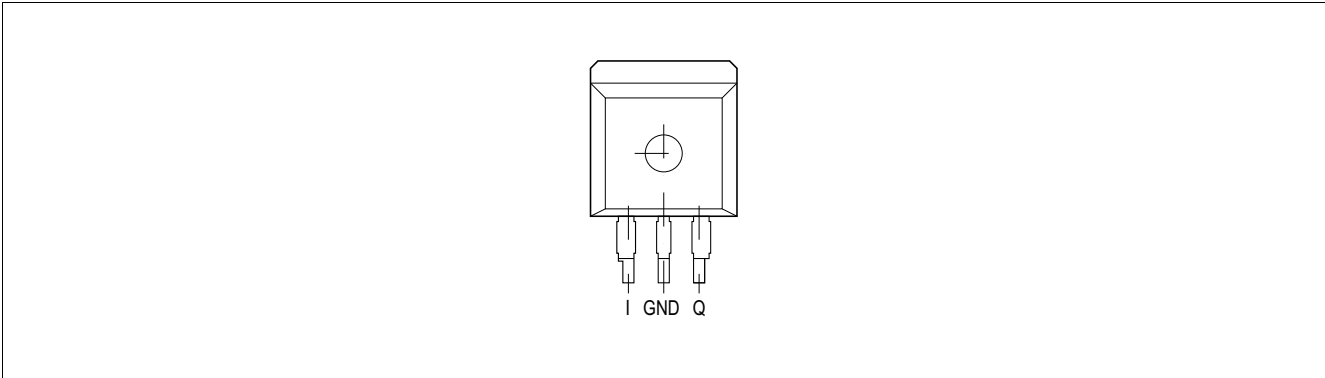


**Figure 1** Block diagram

**Pin configuration**

**2 Pin configuration**

**2.1 Pin assignment**



**Figure 2 Pin configuration**

**2.2 Pin definitions and functions**

**Table 1 Pin definitions and functions**

Pin	Symbol	Function
1	I	<b>Input</b> Block to ground directly at the IC with a ceramic capacitor
2	GND	<b>Ground</b> Internally connected to heat slug
3	Q	<b>Output</b> Block to ground with a capacitor close to the IC terminals, respecting the values given for its capacitance and ESR in <a href="#">Table 3</a>
Heat slug	–	<b>Heat slug</b> Internally connected to GND; connect to GND and heatsink area

### 3 General product characteristics

#### 3.1 Absolute maximum ratings

**Table 2 Absolute maximum ratings<sup>1)</sup>**

$T_j = -40^{\circ}\text{C}$  to  $+150^{\circ}\text{C}$ , all voltages with respect to ground, (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Input I							
Voltage	$V_I$	-42	–	45	V	–	P_4.1.1
Output Q							
Voltage	$V_Q$	-1	–	40	V	–	P_4.1.2
Temperature							
Junction temperature	$T_j$	-40	–	150	°C	–	P_4.1.3
Storage temperature	$T_{\text{stg}}$	-50	–	150	°C	–	P_4.1.4
ESD susceptibility							
ESD absorption	$V_{\text{ESD,HBM}}$	-4	–	4	kV	<sup>2)</sup> Human body model (HBM)	P_4.1.5
ESD absorption	$V_{\text{ESD,CDM}}$	-1000	–	1000	V	<sup>3)</sup> Charge device model (CDM) at all pins	P_4.1.6

1) Not subject to production test, specified by design.

2) ESD susceptibility human body model (HBM) according to AEC-Q100-002 - JESD22-A114.

3) ESD susceptibility charged device model (CDM) according to ESDA STM5.3.1.

#### Notes

1. Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. Integrated protection functions are designed to prevent IC destruction under fault conditions described in the datasheet. Fault conditions are considered as “outside” normal operating range. Protection functions are not designed for continuous repetitive operation.

**General product characteristics**

### 3.2 Functional range

**Table 3 Functional range**

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Input voltage	$V_I$	5.5	–	40	V		P_4.2.1
Output capacitor's requirements for stability	$C_Q$	22		–	$\mu\text{F}$	<sup>1)</sup>	P_4.2.3
Output capacitor's requirements for stability	$ESR(C_Q)$	–		3	$\Omega$	<sup>2)</sup>	P_4.2.4
Junction temperature	$T_j$	-40		150	$^{\circ}\text{C}$	–	P_4.2.5

1) The minimum output capacitance requirement is applicable for a worst-case capacitance tolerance of 30%.

2) Relevant ESR value at  $f = 10 \text{ kHz}$ .

**Note:** Within the functional or operating range, the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the Electrical Characteristics table.

### 3.3 Thermal resistance

**Note:** This thermal data was generated in accordance with JEDEC JESD51 standards. For more information, go to [www.jedec.org](http://www.jedec.org).

**Table 4 Thermal resistance<sup>1)</sup>**

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Junction to case	$R_{thJC}$	–	3.6	–	K/W	Measured to heat slug	P_4.3.6
Junction to ambient	$R_{thJA}$	–	22	–	K/W	<sup>2)</sup> FR4 2s2p board	P_4.3.7
Junction to ambient	$R_{thJA}$	–	74	–	K/W	<sup>3)</sup> FR4 1s0p board, footprint only	P_4.3.8
Junction to ambient	$R_{thJA}$	–	42	–	K/W	<sup>3)</sup> FR4 1s0p board, 300 mm <sup>2</sup> heatsink area	P_4.3.9
Junction to ambient	$R_{thJA}$	–	34	–	K/W	<sup>3)</sup> FR4 1s0p board, 600 mm <sup>2</sup> heatsink area	P_4.3.10

1) Not subject to production test, specified by design.

2) The specified  $R_{thJA}$  value is according to JEDEC JESD51-2,-5,-7 at natural convection on an FR4 2s2p board. The product (chip and package) was simulated on a  $76.2 \times 114.3 \times 1.5 \text{ mm}^3$  board with two inner copper layers ( $2 \times 70 \mu\text{m Cu}$ ,  $2 \times 35 \mu\text{m Cu}$ ). Where applicable, a thermal via array under the exposed pad contacted the first inner copper layer.

3) The specified  $R_{thJA}$  value is according to JEDEC JESD 51-3 at natural convection on an FR4 1s0p board. The product (chip and package) was simulated on a  $76.2 \times 114.3 \times 1.5 \text{ mm}^3$  board with one copper layer ( $1 \times 70 \mu\text{m Cu}$ ).

## Electrical characteristics

### 4 Electrical characteristics

#### 4.1 Electrical characteristics of the voltage regulator

**Table 5 Electrical characteristics**

$V_I = 13.5 \text{ V}$ ,  $T_j = -40^\circ\text{C}$  to  $+150^\circ\text{C}$ ; all voltages with respect to ground (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Output Q							
Output voltage	$V_Q$	4.9	5.0	5.1	V	5 mA < $I_Q$ < 400 mA; 6 V < $V_I$ < 28 V	P_5.1.1
Output voltage	$V_Q$	4.9	5.0	5.1	V	5 mA < $I_Q$ < 200 mA; 6 V < $V_I$ < 40 V	P_5.1.2
Dropout voltage	$V_{dr}$	–	250	500	mV	<sup>1)</sup> $I_Q$ = 250 mA; $V_{dr}$ = $V_I$ – $V_Q$	P_5.1.5
Load regulation	$\Delta V_{Q, lo}$	–	20	50	mV	$I_Q$ = 5 mA to 400 mA; $V_I$ = 6 V	P_5.1.6
Line regulation	$\Delta V_{Q, li}$	–	10	25	mV	$V_I$ = 12 V to 32 V; $I_Q$ = 5 mA	P_5.1.8
Output current limitation	$I_Q$	400	600	1100	mA	<sup>1)</sup>	P_5.1.9
Power supply ripple rejection	$PSRR$	–	60	–	dB	<sup>2)</sup> $f_r$ = 100 Hz; $V_r$ = 0.5 Vpp	P_5.1.10
Temperature output voltage drift	$\frac{dV_Q}{dT}$	–	0.5	–	mV/K	–	P_5.1.11
Overtemperature shutdown threshold	$T_{j, sd}$	151	–	200	°C	<sup>2)</sup> $T_j$ increasing	P_5.1.12
Overtemperature shutdown threshold hysteresis	$T_{j, sdh}$	–	25	–	°C	<sup>2)</sup> $T_j$ decreasing	P_5.1.13
Current consumption							
Quiescent current $I_q = I_I - I_Q$	$I_q$	–	100	220	μA	$I_Q$ = 1 mA	P_5.1.14
Current consumption $I_q = I_I - I_Q$	$I_q$	–	8	15	mA	$I_Q$ = 250 mA	P_5.1.15
Current consumption $I_q = I_I - I_O$	$I_q$	–	15	25	mA	$I_Q$ = 400 mA	P_5.1.16

1) Measured when the output voltage  $V_Q$  has dropped 100 mV from the nominal value obtained at  $V_I = 13.5 \text{ V}$ .

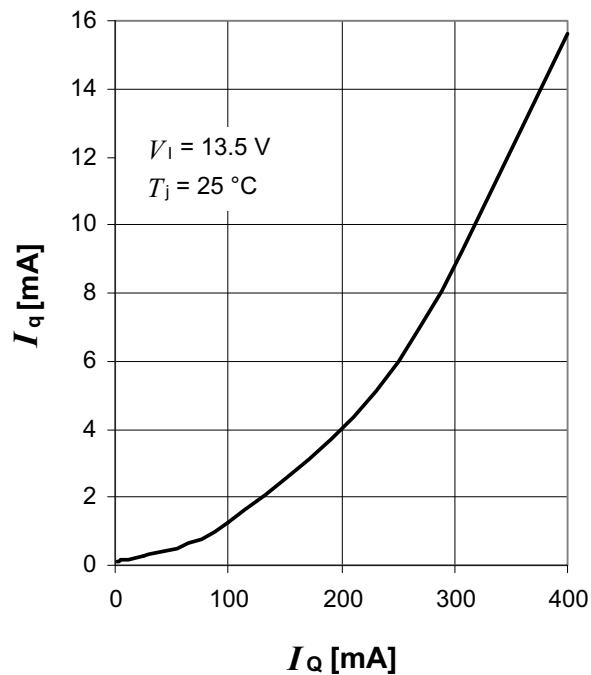
2) Not subject to production test, specified by design.

Typical performance characteristics

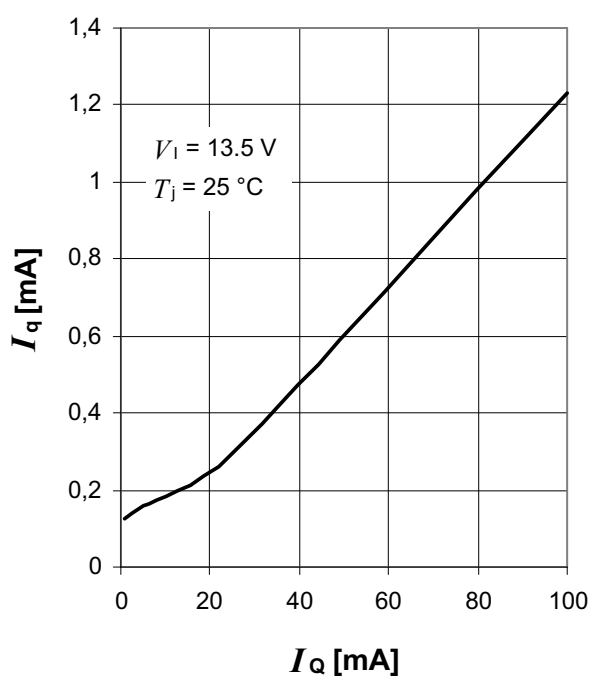
## 5 Typical performance characteristics

### 5.1 Typical performance characteristics of the voltage regulator

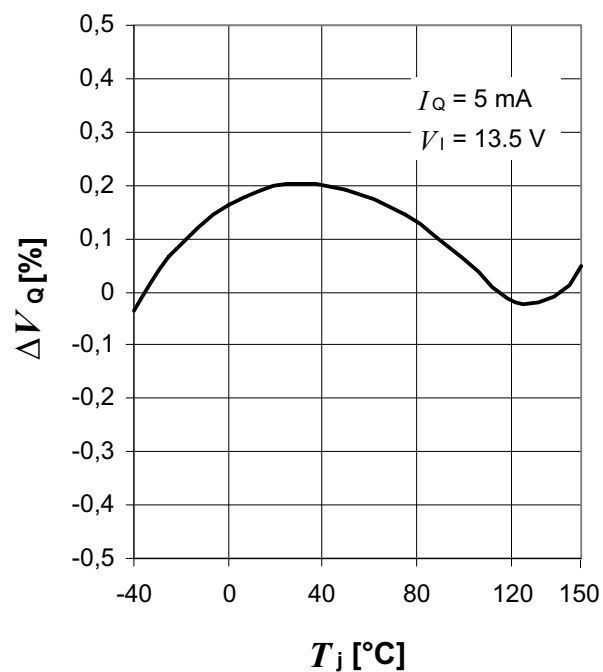
**Current consumption  $I_q$  versus output current  $I_Q$**



**Current consumption  $I_q$  versus low output current  $I_Q$**



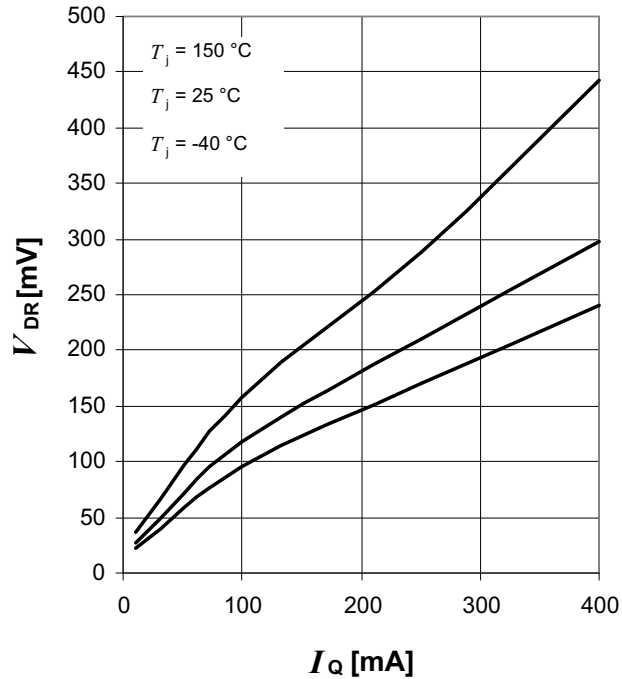
**Output voltage variation  $\Delta V_Q$  versus junction temperature  $T_j$**



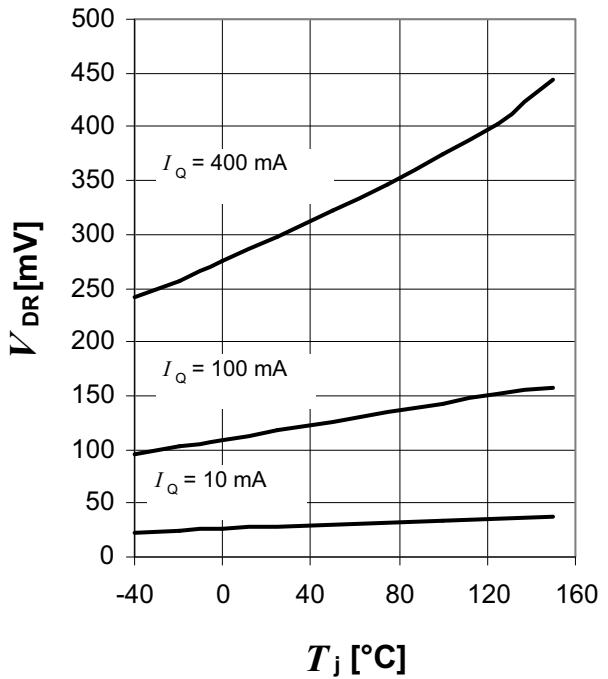


**Typical performance characteristics**

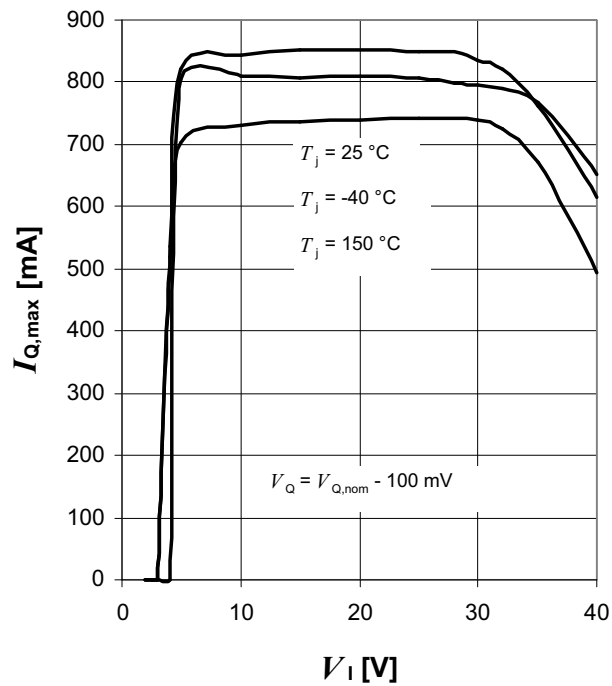
**Dropout voltage  $V_{dr}$  versus output current  $I_Q$**



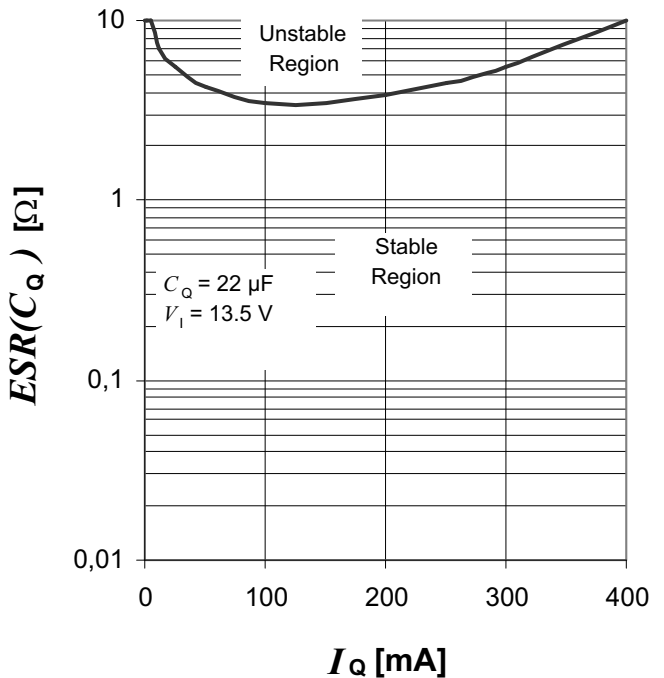
**Dropout voltage  $V_{dr}$  versus junction temperature**



**Maximum output current  $I_{Q,max}$  versus input voltage  $V_I$**



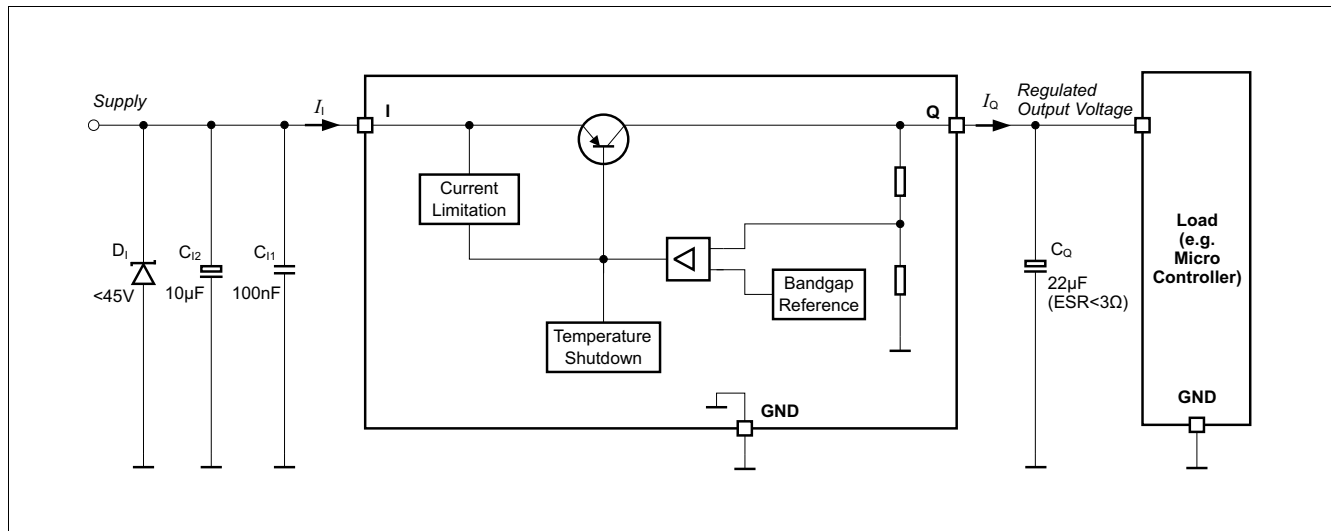
**Region of stability: output capacitor's  $ESR(C_Q)$  versus output current  $I_Q$**



## Application information

## 6 Application information

**Note:** The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition, or quality of the device.



**Figure 3** Application diagram

**Note:** This is a very simplified example of an application circuit. The function must be verified in the real application.

### 6.1 Selection of external components

#### 6.1.1 Input pin

The typical input circuitry for a linear voltage regulator is shown in [Figure 3](#).

A ceramic capacitor at the input, in the range of 100 nF to 470 nF, is recommended to filter out the high frequency disturbances imposed by the line, for example, ISO pulses 3a/b. This capacitor must be placed very close to the input pin of the linear voltage regulator on the PCB.

An aluminum electrolytic capacitor in the range of 10 µF to 470 µF is recommended as an input buffer to smooth out high energy pulses, such as ISO pulse 2a. This capacitor should be placed close to the input pin of the linear voltage regulator on the PCB.

An overvoltage suppressor diode can be used to further suppress any high voltage beyond the maximum rating of the linear voltage regulator and protect the device against any damage due to overvoltage.

The external components at the input are not mandatory for the operation of the voltage regulator, but they are recommended in case of possible external disturbances.

#### 6.1.2 Output pin

An output capacitor is mandatory for the stability of linear voltage regulators.

The requirement to the output capacitor is given in [Table 3](#). The graph [Region of stability: output capacitor's ESR\(C<sub>Q</sub>\) versus output current I<sub>Q</sub>](#) shows the stable operation range of the device.

## Application information

The TLE42744GV50 is designed to be stable with extremely low-ESR capacitors. According to the automotive environment, ceramic capacitors with X5R or X7R dielectrics are recommended.

The output capacitor should be placed as close as possible to the regulator's output and GND pins, and on the same side of the PCB as the regulator itself.

In case of rapid transients of input voltage or load current, the capacitance should be dimensioned in accordance, and verified in the real application that the output stability requirements are fulfilled.

## 6.2 Thermal considerations

Knowing the input voltage, the output voltage, and the load profile of the application, the total power dissipation can be calculated:

(6.1)

$$P_D = (V_I - V_Q) \times I_Q + V_I \times I_q$$

with

- $P_D$ : continuous power dissipation
- $V_I$ : input voltage
- $V_Q$ : output voltage
- $I_Q$ : output current
- $I_q$ : quiescent current

The maximum acceptable thermal resistance  $R_{thJA}$  can then be calculated:

(6.2)

$$R_{thJA, \max} = \frac{T_{j, \max} - T_a}{P_D}$$

with

- $T_{j, \max}$ : maximum allowed junction temperature
- $T_a$ : ambient temperature

Based on the above calculation, the proper PCB type and the necessary heat sink area can be determined with reference to the specification in [Table 4](#).

### Example

Application conditions:

$$V_I = 13.5 \text{ V}$$

$$V_Q = 5 \text{ V}$$

$$I_Q = 250 \text{ mA}$$

$$T_a = 85^\circ\text{C}$$

## Application information

Calculation of  $R_{thJA,max}$ :

$$\begin{aligned}P_D &= (V_I - V_Q) \times I_Q + V_I \times I_q \\&= (13.5 \text{ V} - 5 \text{ V}) \times 250 \text{ mA} + 13.5 \text{ V} \times 15 \text{ mA} \\&= 2.125 \text{ W} + 0.2025 \text{ W} \\&= 2.3275 \text{ W}\end{aligned}$$

$$\begin{aligned}R_{thJA,max} &= (T_{j,max} - T_a) / P_D \\&= (150^\circ\text{C} - 85^\circ\text{C}) / 2.3275 \text{ W} \\&= 27.93 \text{ K/W}\end{aligned}$$

As a result, the PCB design must ensure a thermal resistance  $R_{thJA}$  lower than 27.93 K/W. By considering the thermal resistance as provided in [Table 4](#), a FR4 2s2p board is required in this case.

### 6.3 Reverse polarity protection

The TLE42744GV50 is self-protected against reverse-polarity faults and allows negative supply voltage. External reverse-polarity diode is not needed. However, the absolute maximum ratings of the device as specified in [Table 2](#) must be kept.

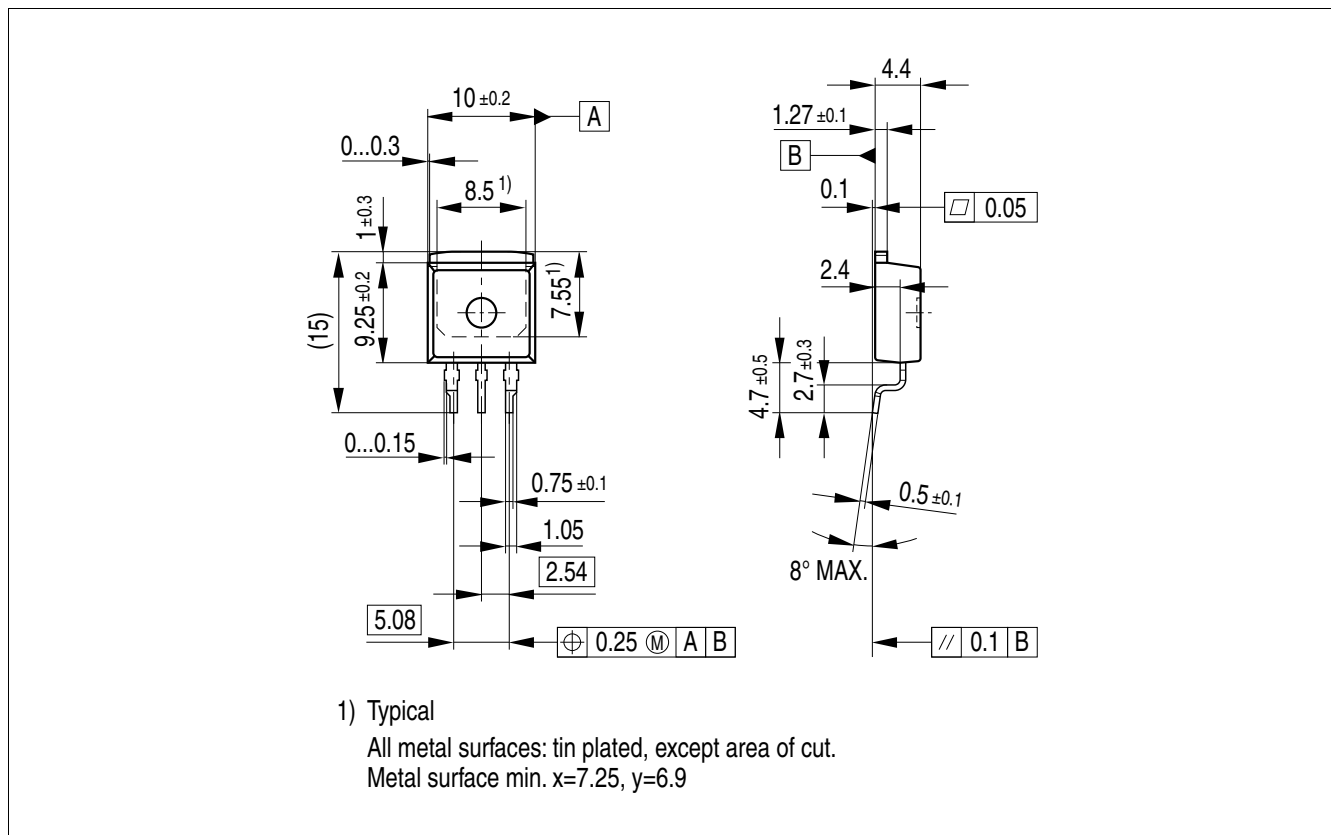
The reverse voltage causes several small currents to flow into the IC hence increasing its junction temperature. As the thermal-shutdown circuitry does not work in the reverse polarity condition, designers have to consider this in their thermal design.

### 6.4 Further application information

For further information, visit <https://www.infineon.com>.

**Package information**

## 7 Package information



**Figure 4 PG-T0263-3<sup>1)</sup>**

### Green Product (RoHS-compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a Green Product. Green Products are RoHS-compliant (Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

### Further information on packages

<https://www.infineon.com/packages>

1) Dimensions in mm

**Revision history**

## **8 Revision history**

<b>Revision</b>	<b>Date</b>	<b>Changes</b>
1.4	2025-02-01	Separation of the TLE42744 rev. 1.30 datasheet into individual product offerings Template update and editorial changes
1.3	2018-03-05	Marking update in chapter overview (TLE42744GSV33 and TLE42744DV33) Updated template on the last page
1.2	2014-07-03	Application information added PG-TO252-3 and PG-SSOP-14 EP package outlines updated
1.1	2010-01-13	Updated version datasheet: version TLE42744EV50 in PG-SSOP-14 exposed pad and all related description added; 3.3 V versions TLE42744GV33 in PG-TO263-3, TLE42744DV33 in PG-TO252-3 and TLE42744GSV33 in PG-SOT223-4 and all related description added
1.0	2009-01-14	Initial version final datasheet

#### Trademarks

All referenced product or service names and trademarks are the property of their respective owners.

**Edition 2025-02-01**

**Published by**

**Infineon Technologies AG**

**81726 Munich, Germany**

**© 2025 Infineon Technologies AG.**

**All Rights Reserved.**

**Do you have a question about any aspect of this document?**

**Email: [erratum@infineon.com](mailto:erratum@infineon.com)**

**Document reference**

**Z8F80588455**

#### IMPORTANT NOTICE

The information given in this document shall in no event be regarded as a guarantee of conditions or characteristics ("Beschaffenheitsgarantie").

With respect to any examples, hints or any typical values stated herein and/or any information regarding the application of the product, Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind, including without limitation warranties of non-infringement of intellectual property rights of any third party.

In addition, any information given in this document is subject to customer's compliance with its obligations stated in this document and any applicable legal requirements, norms and standards concerning customer's products and any use of the product of Infineon Technologies in customer's applications.

The data contained in this document is exclusively intended for technically trained staff. It is the responsibility of customer's technical departments to evaluate the suitability of the product for the intended application and the completeness of the product information given in this document with respect to such application.

For further information on technology, delivery terms and conditions and prices, please contact the nearest Infineon Technologies Office ([www.infineon.com](http://www.infineon.com)).

#### WARNINGS

Due to technical requirements products may contain dangerous substances. For information on the types in question please contact your nearest Infineon Technologies office.

Except as otherwise explicitly approved by Infineon Technologies in a written document signed by authorized representatives of Infineon Technologies, Infineon Technologies' products may not be used in any applications where a failure of the product or any consequences of the use thereof can reasonably be expected to result in personal injury.